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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,840	07/10/2003	Jong-Woo Kim	053785-5018-02	8882

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MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
CHUNG, DAVID Y	
ART UNIT	PAPER NUMBER
2871	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,840	KIM ET AL.	
	Examiner	Art Unit	
	DAVID Y. CHUNG	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/885,527.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6, 8-13, and 15-17 rejected under 35 U.S.C. 102(a) as being unpatentable over Park et al. (US 6,335,276) in view of Sasano et al. (US 5,402,254).

As to claim 1, Park discloses a method for manufacturing a thin film transistor array for a liquid crystal display and a photolithography method for fabricating thin films. Park et al. discloses the following steps: forming gate lines, gate electrodes, and gate pads on a substrate; depositing a gate insulating layer, semiconductor layer, ohmic contact layer, and conductor layer; patterning the conductor layer and ohmic contact layer to form data lines, source and data electrodes, and data pads; depositing a passivation layer; coating a photoresist on the passivation layer; exposing the photoresist to light through one or more masks having different transmittance between the display area and peripheral area to form a photoresist pattern having different thickness depending on the position. See abstract. Figure 11 shows a mask with light

shielding portions, light transmissive portions and semi-transmissive portions. Figure 12A shows a photoresist pattern with varying thickness depending on position. Figure 19 shows the active matrix substrate after patterning the passivation layer, active layer and insulating layer and after forming the pixel electrode. Figure 5 shows a cross section of the storage capacitor. Note the first capacitor electrode 22 and the second capacitor electrode 68. Figure 12A shows the photoresist pattern PR comprising region A exposed to light through the light shielding portion of the mask, region B exposed to light through the light transmissive portions of the mask, and region C exposed to light through the semi-transmissive portions of the mask.

Park does not does not disclose a second insulating layer. However, Sasano teaches forming a gate insulating film constituted by a first insulating film and a second insulating film. See column 2, lines 30-32. Sasano teaches that a gate insulating layer constituted by a first insulating layer and a second insulating layer can prevent short-circuiting between electrodes at the thin film transistor. See column 2, lines 57-61. It would have been obvious to one of ordinary skill in the art at the time of invention to form a gate insulating layer constituted by a first insulating layer and a second insulating layer in order to prevent short-circuiting between electrodes at the thin film transistor as taught by Sasano.

As to claim 2, figure 18 shows the gate lines arranged perpendicular to the data lines to form a matrix pattern with the source electrode spaced apart from drain electrode.

As to claim 3, Park discloses depositing and patterning a first conductive layer to form gate wiring by dry or wet etch using a first photolithography step as shown in figures 6A to 6C. See column 10, lines 13 – 18.

As to claims 4 and 5, Park discloses depositing a gate insulator layer (first and second insulating layers as taught by Sasano), semiconductor layer, and second conductive layer and then patterning the second conductive layer to form data wiring and storage capacitor electrodes by a second photolithography step as shown in figures 7A and 7B. See column 10, lines 19 – 34.

As to claim 6, Park discloses patterning the passivation layer, semiconductor layer, and gate insulator to form contact holes 71, 72, and 73 by a third photolithography step as shown in figures 8A, 13A and 13B. For this purpose, a photoresist pattern is formed to have thickness that varies depending on the location. See column 10, lines 35 – 53.

As to claim 8, Park teaches that it is preferable for the thin portions of the photoresist pattern to have a thickness in the range of 350 to 10,000 angstroms. See column 12, lines 21 – 23.

As to claim 9, Park teaches that the gate wiring may have a multi-layered structure, in which case it is preferably made of one material having low resistivity and another material having good contact with other materials. Double layers of Cr/Al (or Al alloy) and Al/Mo are examples given by Park. See column 8, lines 31 – 38.

As to claims 10 and 11, Park teaches that both the gate insulator 30 (first and second insulating layers as taught by Sasano) and passivation layer 70 can be made of inorganic material such as silicon nitride. See column 8, lines 39 – 40 and column 9, lines 45 – 50.

As to claims 12 and 13, Park teaches that the passivation layer can be made of insulating material such as acrylic organic material. See column 9, lines 45 – 50.

As to claims 15 and 16, Park discloses in figure 11, a mask having pattern layer 520. This layer is the same as the opaque pattern layer 320 shown in figure 9A. This layer is made of such material as chromium. See column 11, lines 5 – 10 and 30 – 40.

As to claim 17, Park does not disclose molybdenum silicide material for the transmittance control layer 550 in figure 11. However, molybdenum silicide was a common and conventional semi-transmissive material used in photomasks. It was well known and obvious for transmitting a suitably small percentage of light for most photolithography applications. This allowed the difference between light and dark areas

on the photoresist to be accentuated properly. Therefore, it would have been obvious to one of ordinary skill in the art to form the transmittance control layer in the mask of Park using molybdenum silicide in order to properly accentuate the difference between light and dark areas on the photoresist layer.

2. Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US 6,335,276) in view of Sasano et al. (US 5,402,254) and in further view of Kim (US 6,255,130) and Park et al. (US 6,287,899).

Park (U.S. 6,335,276) discloses data contact holes 73 and gate contact holes 72 formed in passivation layer 70. See figures 3 and 4.

Although Park (U.S. 6,335,276) does not disclose a contact hole formed over storage capacitor electrode 68, Kim discloses a similar device with contact holes connecting the storage capacitor electrode to the pixel electrode. Note contact holes 74 in figures 1 and 2. It was well known and obvious that this would increase the storage capacitance and lead to better aperture ratio. Therefore, it would have been obvious to one of ordinary skill in the art to connect the storage capacitor to the pixel electrode via contact holes in the passivation layer in order to improve aperture ratio.

Although Park (U.S. 6,335,276) does not disclose exposing both a side portion and upper surface of the drain electrode, it was well known and obvious to do this in order to increase the contact area and form better electrical connection between the pixel electrode and drain electrode as shown in figure 15 of Park (U.S. 6,287,889).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to expose both a side portion and upper surface of the drain electrode in order to form better electrical contact with the pixel electrode.

3. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US 6,335,276) in view of Sasano et al. (US 5,402,254) and in further view of Park et al. (US 6,287,899).

Park (U.S. 6,335,276) does not disclose making the width of the passivation layer smaller than the width of the data line. However, Park (U.S. 6,287,899) discloses a redundant data line overlapping and connecting to the primary data line through a contact hole. See figure 4. It was well known and obvious that making the width of the passivation layer smaller than the width of the data line caused the side portions of the data line to be exposed. It was well known and obvious that exposing side portions of the data line increased contact area and improved the electrical connection to the data line. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to make the width of the passivation layer smaller than the width of the data line in order to improve electrical connection between the primary data line and a redundant data line.

Response to Arguments

Applicant's arguments filed June 11, 2008 have been fully considered but they are not persuasive. Applicant has amended claim 1 to recite that first photoresist portions correspond to portions of the TFT, data line, and second capacitor electrode; second photoresist portions correspond to portions of the gate pad, data pad, and second capacitor electrode; and third photoresist portions correspond to the pixel region, and portions of the gate pad, source electrode and drain electrode. Applicant has argued that this distinguishes the claim from the prior art of Park (US 6,335,276). However, without further distinguishing the first, second and third photoresist portions from one another, any part of the photoresist layer disclosed by Park (US 6,335,276) can be construed as the first, second, and third photoresist portions including the parts which correspond to what is claimed for each. Therefore, the amended claim is still unpatentable over the prior art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Y. Chung whose telephone number is (571) 272-2288. The examiner can normally be reached Monday thru Friday from 8:30 am to 5:00 pm. If successive attempts to contact the examiner are unsuccessful, the examiner's supervisor David C. Nelms can be reached at (571) 272-1787.

/David Y. Chung/

Examiner, Art Unit 2871

/David Nelms/

Supervisory Patent Examiner, Art Unit 2871